RCETECAC02 - Digital Circuit design

Course outcomes:

- Be able to manipulate numeric information in different forms
- Be able to manipulates impleBoolean expressions using the theorems and postulates of Boolean algebra and to minimize combinational functions.
- Beabletodesignandanalyzesmallcombinationalcircuitsandtousestandardcombinationalfuncti ons to build larger more complex circuits.
- Beabletodesignandanalyzesmallsequentialcircuitsandtousestandardsequentialfunctionsto build larger more complex circuits.

Syllabus:

UNIT I

Number System and Boolean Algebra:

Number Systems, Base Conversion Methods, Complements of Numbers, Codes- Binary Codes, Binary Coded Decimal Code and its Properties, Unit Distance Codes, Error Detecting and Correcting Codes. Digital Logic Gates (AND, NAND,OR,NOR,EX-OR,EX-NOR), Properties of XOR Gates, Universal Gates, Basic Theorems and Properties, Switching Functions, Canonical and Standard Form.

UNIT II

Minimization Techniques:

Introduction, The minimization with theorems, The Karnaugh Map Method, Three, Four and Five variable K- Maps, Prime and Essential Implications, Don't Care Map Entries, Using the Maps for Simplifying, Quine-McCluskey Method, Multilevel NAND/NOR realizations.

UNIT III

Combinational Circuits:

Design Procedure – Half Adder, Full Adder, Half Subtractor, Full Subtractor, Parallel Binary Adder, Parallel binary subtractor, Binary Multiplier, Multiplexers/DeMultiplexers, decoder, Encoder, Code Converters, Magnitude Comparator. classification of sequential circuits, The

binary cell, The S-R-Latch Flip-Flop The D-Latch Flip-Flop, The "Clocked T" Flip-Flop, The "Clocked J-K" Flip-Flop, Design of a Clocked Flip-Flop, Timing and Triggering Consideration

UNIT IV

Sequential Circuits:

Introduction, Basic Architectural Distinctions between Combinational and Sequential circuits, Latches, Flip-Flops, SR, JK, D, T and Master slave, characteristic Tables and equations, Conversion from one type of Flip-Flop to another, Counters - Design of Single Mode Counter, Ripple Counter, Ring Counter, Shift Register, Ring counter using Shift Register

UNIT V

Memory Devices:

Classification of memories – ROM: ROM organization, PROM, EPROM,EEPROM, RAM:RAMorganization,Writeoperation,Readoperation,StaticRAM,ProgrammableLogicDevices:ProgrammableLogicArray(PLA),ProgrammableArrayLogic,ImplementationofCombinational Logic circuits using ROM, PLA, PAL.

Reference Text Books:

1. Introduction to Switching Theory and Logic Design – Fredriac J. Hill, Gerald R. Peterson, 3rd Ed,John Wiley & Sons Inc.
2. Digital Fundamentals – A Systems Approach – Thomas L. Floyd, Pearson, 2013.
3. Switching Theory and Logic Design – Bhanu Bhaskara –Tata McGraw Hill Publication, 2012
4. Fundamentals of Logic Design- Charles H. Roth, Cengage Leanring, 5th, Edition, 2004.
5. Digital Logic Applications and Design- John M. Yarbrough, Thomson Publications, 2006.
6. Digital Logic and State Machine Design – Comer, 3rd, Oxford, 2013.